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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/630,504	07/30/2003	Jane Xin-LeBlanc	P05725	7910

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EXAMINER	
NATALINI, JEFF WILLIAM	
ART UNIT	**PAPER NUMBER**
2858	

DATE MAILED: 09/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/630,504	XIN-LEBLANC ET AL.	
	Examiner	Art Unit	
	Jeff Natalini	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 11-13* is/are rejected.

7)☒ Claim(s) *4-10 and 14-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 February 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

1. The specification is objected to because of the following informalities:

- On pg 1 line 7-8, please delete Docket No. NATI15-05644 and replace with 10/630322.
- On pg 1 line 11-12 please delete Docket No. NATI15-00037 and replace with 10/630311.
- On pg 1 line 15 please delete Docket No. NATI15-05644 and replace with 10/630322.
- On pg 1 line 16 please delete Docket No. NATI15-00037 and replace with 10/630311.
- On pg 10 line 15 frequency divider (160) should read frequency divider (150) as there is no reference to a 160 in the drawings.
- On pg 18 line 22-23 and pg 19 line 1 it is stated, "When precharge = 0, P-channel transistor 423 is off, but P-Channel transistor 423 is still on." This would lead one to assume transistor 423 is off and on at the same time, which is an incorrect assessment of the situation.

Appropriate correction is required.

Drawings

2. Figure 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled

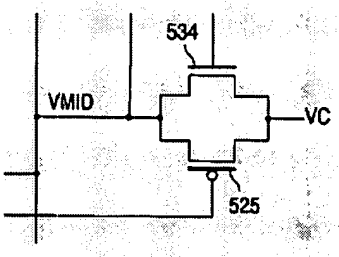
"Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "second impedance circuit coupled between said first internal node and a ground rail, wherein said first and second impedance circuits form a voltage divider circuit that biases said first internal node to a target bias voltage when said test signal is disabled" as claimed in claim 4 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

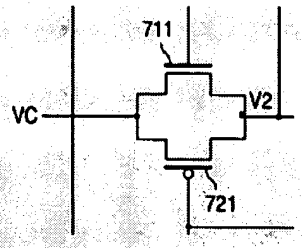
Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of

the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Other formalities with the drawings as follows:



This is from fig 5:
In the specification pg 21 line 14-18, it is disclosed that the source of transistor 534 is coupled to the VMID node, and the drain is coupled to the VC node.



This is from fig 7:
As claimed the drain of transistor 711 is connected to the high impedance node (VC) and the source is connected to the first internal node (V2).

So it is seen the applicant has switched the transistors drain and source terminals as disclosed in two different figures. Please correct all drawings so the drain and source terminals are not switched or provide some arrow or other indication thus allowing one skilled in the art to easily identify the drain and source terminals.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art in view of Balamurugan et al. (6320795).

In regard to claim 1, Admitted prior art discloses a test circuit comprising: a first transmission gate switch (Fig 6 (11)) for coupling high impedance node (VC) to a first internal node (V1) of said test circuit when said test signal is enabled (On), said first transmission gate switch comprising a first N-channel transistor (611) having a drain coupled to said high impedance node (VC), a gate coupled to a Logic 1 when said test signal is enabled (on goes into transistor 611), and a source coupled to said first internal node (V1); a second transmission gate switch capable of coupling said first internal node to a second internal node of said test circuit when test signal is enabled (612).

Admitted prior art lacks a third transmission gate switch capable of coupling said second internal node to said external test point when said test signal is enabled; and a biasing circuit for generating a negative Vgs bias on said first N-channel transistor when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor.

MPEP 2144.04 VI B states that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

Balamurugan et al. teaches a biasing circuit (fig 3 (72)) for generating a negative Vgs bias (col 6 line 20-27) on said first N-channel transistor (fig 3 (62))

when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor (col 7 line 25-30).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for the admitted prior art to include a third transmission gate switch capable of coupling said second internal node to said external test point when said test signal is enabled and a biasing circuit for generating a negative Vgs bias on said first N-channel transistor when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor as taught by MPEP2144.04 VI B and Balamurugan et al. in order to avoid the negative impact on circuit robustness a leakage current provides (col 1 line 20-22).

In regard to claim 2, admitted prior art discloses wherein said first transmission gate switch comprises a first P-channel transistor (fig 6 (621)) having a drain coupled to said high impedance node (VC), a gate coupled to a Logic 0 when said test signal is enabled (On* goes into 621), and a source coupled to said first internal node (V1).

In regard to claim 3, admitted prior art lacks wherein the biasing circuit generates a positive Vgs bias on said first P-channel transistor when said test signal is disabled to thereby reduce leakage current in said first P-channel transistor.

Balamurugan et al. teaches a biasing circuit (fig 3 (72)) for generating a negative Vgs bias (col 6 line 20-27) on said first N-channel transistor (fig 3 (62))

when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor (col 7 line 25-30). It is known in the art that a P-channel transistor is biased in the opposite way of a N-channel transistor, so it would be obvious that since both transistors are connected together (forming CMOS) to the same node that was biased by the circuit taught by Balamurugan et al. a positive bias is produced from the Vgs of the Pchannel transistor.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for the admitted prior art to generate a positive Vgs bias on the P-channel transistor when the test signal is disabled to thereby reduce leakage current in the P-channel transistor as taught by Balamurugan et al. in order to avoid the negative impact on circuit robustness a leakage current provides (col 1 line 20-22).

5. Claims 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nilsson (6605935) in view of the admitted prior art and in further view of Balamurugan et al. (6320795).

In regard to claims 11 and 12, Nilsson discloses a PLL circuit (fig 1) comprising: a voltage controlled oscillator (fig 1 (109)); a charge pump (fig 3 (305)) and loop filter (fig 1 (207)) circuit for generating a control voltage capable of controlling said voltage controlled oscillator (col 3 line 3-10);

Nilsson lacks a test circuit capable of connected a high impedance node to external test point when a test signal driving a circuit is enabled comprising; a

first transmission gate switch for coupling high impedance node to a first internal node of said test circuit when said test signal is enabled, said first transmission gate switch comprising a first N-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 1 when said test signal is enabled, and a source coupled to said first internal node; a second transmission gate switch capable of coupling said first internal node to a second internal node of said test circuit when test signal is enabled; and a third transmission gate switch capable of coupling said second internal node to said external test point when said test signal is enabled; and a biasing circuit for generating a negative Vgs bias on said first N-channel transistor when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor; and P-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said first internal node.

Admitted prior art discloses a test circuit connecting a high impedance node (fig 6 (VC)) to an external test point (fig 6 Vext) comprising: a first transmission gate switch (Fig 6 (11)) for coupling high impedance node (VC) to a first internal node (V1) of said test circuit when said test signal is enabled (On), said first transmission gate switch comprising a first N-channel transistor (611) having a drain coupled to said high impedance node (VC), a gate coupled to a Logic 1 when said test signal is enabled (on goes into transistor 611), and a source coupled to said first internal node (V1); a second transmission gate switch

capable of coupling said first internal node to a second internal node of said test circuit when test signal is enabled (612); and a first P-channel transistor (fig 6 (621)) having a drain coupled to said high impedance node (VC), a gate coupled to a Logic 0 when said test signal is enabled (On* goes into 621), and a source coupled to said first internal node (V1).

MPEP 2144.04 VI B states that mere duplication of parts has no patentable significance unless a new and unexpected result is produced. In re Harza, 274 F.2d 669, 124 USPQ 378 (CCPA 1960).

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Nilsson to incorporate a test circuit connecting a high impedance node to an external test point consisting of three transmission gate switches containing two internal nodes between them and the first switch comprising of a N-channel transistor with drain connected to high impedance, gate to test signal, and source to the first internal node; and a P-channel transistor having a drain coupled to said high impedance node, a gate coupled to a Logic 0 when said test signal is enabled, and a source coupled to said first internal node as taught by the admitted prior art and MPEP 2144.04 VI B in order to provide for measurement purposes (specification pg 22 line 3-5).

Balamurugan et al. teaches a biasing circuit (fig 3 (72)) for generating a negative Vgs bias (col 6 line 20-27) on said first N-channel transistor (fig 3 (62)) when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor (col 7 line 25-30). It is known in the art that a P-channel

transistor is biased in the opposite way of a N-channel transistor, so it would be obvious that since both transistors are connected together (forming CMOS) to the same node that was biased by the circuit taught by Balamurugan et al. a positive bias is produced from the Vgs of the Pchannel transistor.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Nilsson to generate a positive Vgs bias on the P-channel transistor when the test signal is disabled to thereby reduce leakage current in the P-channel transistor as taught by Balamurugan et al. in order to avoid the negative impact on circuit robustness a leakage current provides (col 1 line 20-22).

In regard to claim 13, Nilsson and admitted prior art lacks wherein the biasing circuit generates a positive Vgs bias on said first P-channel transistor when said test signal is disabled to thereby reduce leakage current in said first P-channel transistor.

Balamurugan et al. teaches a biasing circuit (fig 3 (72)) for generating a negative Vgs bias (col 6 line 20-27) on said first N-channel transistor (fig 3 (62)) when said test signal is disabled to thereby reduce leakage current in said first N-channel transistor (col 7 line 25-30). It is known in the art that a P-channel transistor is biased in the opposite way of a N-channel transistor, so it would be obvious that since both transistors are connected together (forming CMOS) to the same node that was biased by the circuit taught by Balamurugan et al. a positive bias is produced from the Vgs of the Pchannel transistor.

It would have been obvious to one with ordinary skill in the art at the time the invention was made for Nilsson and the admitted prior art to generate a positive Vgs bias on the P-channel transistor when the test signal is disabled to thereby reduce leakage current in the P-channel transistor as taught by Balamurugan et al. in order to avoid the negative impact on circuit robustness a leakage current provides (col 1 line 20-22).

Allowable Subject Matter

6. Claims 4-10 and 14-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

With regard to claim 4 and 14 the prior art does not teach or render obvious wherein "the bias circuit comprising a first impedance circuit coupled between the first internal node and VDD power rail and a second impedance circuit coupled between the same internal node and a ground rail, thus forming a voltage divider that biases the first internal node" and combination as claimed.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rose et al. (5583821) teaches a pass transistor that recieves a reverse bias voltage to switch the pass transistor into a non-conducting state, where the reverse bias substantially reduces the leakage current through the pass transistor.

Houston (5917365) teaches varying the voltage bias to a common substrate in order to reduce leakage current in an integrated circuit standby mode. Johnston et al. (5892377) teaches including three additional transistors to the existing path to eliminate leakage current.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeff Natalini whose telephone number is 571-272-2266. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Le can be reached on 571-272-2233. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeff Natalini

ANJAN DEB
PRIMARY EXAMINER